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Top 17 VLSI Interview Questions & Answers 1) Explain how logical gates are controlled by Boolean logic? In Boolean algebra, the true state is denoted by the number one, referred as logic one or logic high. While, the false state is represented by the number zero,

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called logic zero or logic low.

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Question2: What are the various regions of operation of MOSFET? How are those regions used? Question3: What is threshold voltage?

Question4: What does it mean 'the channel is pinched off'?

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VLSI Design Interview Questions . Question 33. What Is Local-skew, Global-skew,useful-skew Mean? Answer : Local skew : The difference between the clock reaching at the launching flop vs the clock reaching the destination flip-flop of a timing-path.

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VLSI Interview Questions and Answers :- 1. Why does the present VLSI circuits use MOSFETs instead of BJTs? Compared to BJTs, MOSFETs can be made very small as they occupy very small silicon area on IC chip and are relatively simple in terms of manufacturing.

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1. What Are Four Generations Of Integration Circuits? Answer :

SSI (Small Scale Integration) MSI (Medium Scale...

SSI (Small Scale Integration) MSI (Medium Scale Integration) LSI (Large

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interview.

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Answer 2. Implement an 2-input AND gate using a 2x1 mux.

Answer 3. What is a multiplexer? Answer A multiplexer is a combinational circuit which selects one of many input signals and directs to the only output. 4. What is a ring counter? Answer A ring counter is a type of counter composed of a circular shift register.

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We are in process to add more questions. If you have any question that can be added to this section then please write to us with Question and detailed answer at info@vlsiencyclopedia.com we would be glad to mention you as contributor. Thanks, Team VLSI

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Here are eight VLSI interview questions and answers that potential hiring managers may ask you during an interview to determine if you're the right fit for the role. 1. Can you point out the two main types of procedural blocks in Verilog? There are two primary types of procedural blocks available in Verilog which are:

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