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Designing Sorting Networks: A New Paradigm provides an in-depth guide to maximizing the efficiency of sorting networks, and uses 0/1 cases, partially ordered sets and Haase diagrams to closely analyze their behavior in an easy, intuitive manner.

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Designing Sorting Networks A New Paradigm

When children are designing their own sorting networks, they should test them with all possibly input patterns. For example, to check a 3-input sorting network, there are 6 (3x2x1) possible input permutations, and for 4 inputs there are 24 (4x3x2x1) permutations, and for n inputs there are n! (factorial) permutations.

Sorting Networks ← Computer Science Unplugged

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Designing Sorting Networks A New Paradigm

I. Sorting Networks (Sorting, Counting, Load Balancing) II. Matrix Multiplication (Serial and Parallel) III. Linear Programming (Formulating, Applying and Solving) IV. Approximation Algorithms: Covering Problems V. Approximation Algorithms via Exact Algorithms VI. Approximation Algorithms: Travelling Salesman Problem VII.

I. Sorting Networks

This video is part of an online course, Intro to Parallel Programming. Check out the course here: https://www.udacity.com/course/cs344.

Sorting Networks Part 1 - Intro to Parallel Programming ...

Abstract. Here we consider N = 2 p where p is a large integer. Thus, we can capitalize on our knowledge of BOOL(N) in order to try to find faster sorting networks for large values of N.Assume that we find a divide-and-conquer method that uses mp steps to reduce the problem of sorting N keys to sorting a number of groups in parallel where each group has no more than N e keys.

Sorting Networks For Large N ¦ SpringerLink
Such networks are typically designed to perform sorting on fixed numbers of values, in which case they are called sorting networks. Sorting networks differ from general comparison sorts in that they are not capable of handling arbitrarily large inputs, and in that their sequence of comparisons is set in advance, regardless of the outcome of previous comparisons. In order to sort larger amounts of inputs, new sorting networks must be constructed.

Sorting network - Wikipedia
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Designing Sorting Networks: A New Paradigm provides an in-depth guide to maximizing the efficiency of sorting networks, and uses 0/1 cases, partially ordered sets and Haase diagrams to closely analyze their behavior in an easy, intuitive manner. This book also outlines new ideas and techniques for designing faster sorting networks using Sortnet, and illustrates how these techniques were used to design faster 12-key and 18-key sorting networks through a series of case studies. Finally, it examines and explains the mysterious behavior exhibited by the fastest-known 9-step 16-key network. Designing Sorting Networks: A New Paradigm is intended for advanced-level students, researchers and practitioners as a reference book. Academics in the fields of computer science, engineering and mathematics will also find this book invaluable.

Sorting networks are cost-effective multistage interconnection networks with sorting capabilities. AKS Sorting networks sort N keys in C(logN) steps, but the constant C is so high as to render these networks impractical. The fastest Sorting networks designed so far use merge-sorting and sort N keys in O((logN)(logN)) steps. A network that sorts 16 keys in 9 steps was discovered by Van Voorhis. This network is faster than the 10-step merge-sorting network for 16 keys. This suggests that networks that are faster than merge-sorting networks can be designed. It is necessary to bridge the gap between the optimal impractical solutions and the practical solutions. This research aims at achieving this goal via finding a technique for designing faster Sorting networks, i.e. networks that require fewer steps than the corresponding merge-sorting networks. A zero/one case is a sequence of N binary keys. Using zero/one cases to help design Sorting networks, is advantageous since it simplifies the sorting task, and helps track the progress of sorting. To help synthesize and analyze Sorting networks, Batcher developed the software tool Sortnet, which utilizes zero/one cases. With the help of Sortnet, a three-phase technique for designing Sorting networks that are faster than the merge-sorting networks was developed. The technique can also be used to design faster sorting programs in parallel processors. This technique is illustrated with two network designs that are faster than the corresponding merge-sorting designs: an 18-key network using only 11 steps and a 22-key network using only 12 steps.

This book suggests and describes a number of fast parallel circuits for data/vector processing using FPGA-based hardware accelerators. Three primary areas are covered: searching, sorting, and counting in combinational and iterative networks. These include the application of traditional structures that rely on comparators/swappers as well as alternative networks with a variety of core elements such as adders, logical gates, and look-up tables. The iterative technique discussed in the book enables the sequential reuse of relatively large combinational blocks that execute many parallel operations with small propagation delays. For each type of network discussed, the main focus is on the step-by-step development of the architectures proposed from initial concepts to synthesizable hardware description language specifications. Each type of network is taken through several stages, including modeling the desired functionality in software, the retrieval and automatic conversion of key functions, leading to specifications for optimized hardware modules. The resulting specifications are then synthesized, implemented, and tested in FPGAs using commercial design environments and prototyping boards. The methods proposed can be used in a range of data processing applications, including traditional sorting, the extraction of maximum and minimum subsets from large data sets, communication-time data processing, finding frequently occurring items in a set, and Hamming weight/distance counters/comparators. The book is intended to be a valuable support material for university and industrial engineering courses that involve FPGA-based circuit and system design.

This book constitutes the proceedings of the 16th International Conference on Integration of Constraint Programming, Artificial Intelligence, and Operations Research, CPAIOR 2019, held in Thessaloniki, Greece, in June 2019. The 34 full papers presented together with 9 short papers were carefully reviewed and selected from 94 submissions. The conference brings together interested researchers from Constraint Programming (CP), Artificial Intelligence (AI), and Operations Research (OR) to present new techniques or applications and to provide an opportunity for researchers in one area to learn about techniques in the others. A main objective of this conference series is also to give these researchers the opportunity to show how the integration of techniques from different fields can lead to interesting results on large and complex problems.

THE CONTEXT OF PARALLEL PROCESSING The field of digital computer architecture has grown explosively in the past two decades. Through a steady stream of experimental research, tool-building efforts, and theoretical studies, the design of an instruction-set architecture, once considered an art, has been transformed into one of the most quantitative branches of computer technology. At the same time, better understanding of various forms of concurrency, from standard pipelining to massive parallelism, and invention of architectural structures to support a reasonably efficient and user-friendly programming model for such systems, has allowed hardware performance to continue its exponential growth. This trend is expected to continue in the near future. This explosive growth, linked with the expectation that performance will continue its exponential rise with each new generation of hardware and that (in stark contrast to software) computer hardware will function correctly as soon as it comes off the assembly line, has its down side. It has led to unprecedented hardware complexity and almost intolerable dev- opment costs. The challenge facing current and future computer designers is to institute simplicity where we now have complexity; to use fundamental theories being developed in this area to gain performance and ease-of-use benefits from simpler circuits; to understand the interplay between technological capabilities and limitations, on the one hand, and design decisions based on user and application requirements on the other.

This book constitutes the refereed proceedings of the 15th Annual International Conference on Combinatorial Optimization and Applications, COCOA 2021, which took place in Tianjin, China, during December 17-19, 2021. The 55 papers presented in this volume were carefully reviewed and selected from 122 submissions. They deal with combinatorial optimization and its applications in general, focusing on algorithms design, theoretical and experimental analysis, and applied research of general algorithmic interest.

Genetic algorithms have been used in science and engineering as adaptive algorithms for solving practical problems and as computational models of natural evolutionary systems. This brief, accessible introduction describes some of the most interesting research in the field and also enables readers to implement and experiment with genetic algorithms on their own. It focuses in depth on a small set of important and interesting topics—particularly in machine learning, scientific modeling, and artificial life—and reviews a broad span of research, including the work of Mitchell and her colleagues. The descriptions of applications and modeling projects stretch beyond the strict boundaries of computer science to include dynamical systems theory, game theory, molecular biology, ecology, evolutionary biology, and population genetics, underscoring the exciting "general purpose" nature of genetic algorithms as search methods that can be employed across disciplines. An Introduction to Genetic Algorithms is accessible to students and researchers in any scientific discipline. It includes many thought and computer exercises that build on and reinforce the reader's understanding of the text. The first chapter introduces genetic algorithms and their terminology and describes two provocative applications in detail. The second and third chapters look at the use of genetic algorithms in machine learning (computer programs, data analysis and prediction, neural networks) and in scientific models (interactions among learning, evolution, and culture; sexual selection; ecosystems; evolutionary activity). Several approaches to the theory of genetic algorithms are discussed in depth in the fourth chapter. The fifth chapter takes up implementation, and the last chapter poses some currently unanswered questions and surveys prospects for the future of evolutionary computation.

This book provides some recent advances in design nanometer VLSI chips. The selected topics try to present some open problems and challenges with important topics ranging from design tools, new post-silicon devices, GPU-based parallel computing, emerging 3D integration, and antenna design. The book consists of two parts, with chapters such as: VLSI design for multi-sensor smart systems on a chip, Three-dimensional integrated circuits design for thousand-core processors, Parallel symbolic analysis of large analog circuits on GPU platforms, Algorithms for CAD tools VLSI design, A multilevel memetic algorithm for large SAT-encoded problems, etc.

These contributions, written by the foremost international researchers and practitioners of Genetic Programming (GP), explore the synergy between theoretical and empirical results on real-world problems, producing a comprehensive view of the state of the art in GP. In this year ’ s edition, the topics covered include many of the most important issues and research questions in the field, such as: opportune application domains for GP-based methods, game playing and co-evolutionary search, symbolic regression and efficient learning strategies, encodings and representations for GP, schema theorems, and new selection mechanisms.The volume includes several chapters on best practices and lessons learned from hands-on experience. Readers will discover large-scale, real-world applications of GP to a variety of problem domains via in-depth presentations of the latest and most significant results.

This volume commemorates Shimon Even, one of founding fathers of Computer Science in Israel, who passed away on May 1, 2004. This Festschrift contains research contributions, surveys and educational essays in theoretical computer science, written by former students and close collaborators of Shimon. The essays address natural computational problems and are accessible to most researchers in theoretical computer science.